REMARKS

Claims 1-43 are all the claims pending in the application. Claims 21-43 have been withdrawn from consideration pursuant to a previously filed Response to Restriction Requirement. Claims 2, 3, 6, 7, 9, 10, 11-13, 15, 16 and 19 stand rejected upon informalities. Claims 1-20 stand rejected on prior art grounds. Applicants respectfully traverse these objections/rejections based on the following discussion.

I. The 35 U.S.C. § 112, First Paragraph, Rejection

Claims 2, 3, 6, 7, 9, 10, 11-13, 15, 16 and 19 stand rejected under 35 U.S.C. § 112, first paragraph. Specifically, the Office Action objects to the first gate and second gate having different doping concentrations, different doping species, different materials, and different thicknesses in claims 3, 6, 7, 11-13, and 19. In addition, the Office Action objects to the first and second gate dielectrics comprising different materials and different thicknesses in claims 9, 10, 15, and 16. The Office Action states that such features are not disclosed in the specification.

In response thereto, Applicants note that page 17, lines 15-22 of the specification describes that the invention grows the top and bottom gates and respective gate dielectrics independently and, therefore, the gates and gate dielectrics may be of different materials and different thicknesses. Also, different doping levels and doping species may be incorporated into

each gate. Thus, asymmetric gates may be fabricated. Therefore, Applicants respectfully submit that the specification does, indeed, describe the claimed features clearly and in a manner to enable one skilled in the relevant art, at the time the application was filed, to understand that the inventors had possession of the claimed invention. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection

II. The Prior Art Rejections

Claims 1, 4, 6-8, 11, 14 and 18-20 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Pfiester (U.S. Patent 5,166,084). Claims 2-3, 9-10, 12-13 and 15-16 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Pfiester. Claims 5 and 17 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Pfiester in view of Uesugi et al. (U.S. Patent 5,708,286) hereinafter "Uesugi." Applicants respectfully traverse these rejections based on the following discussion.

A. The 35 U.S. C. §102(b) Rejection Based on Pfiester

1. The Position In the Office Action

With respect to the rejection of claims 1, 4, 6-8, 11, 14, and 18-20, the Office Action states that Pfiester discloses a transistor (Fig. 4) comprising a channel region (16), a first gate (26) on top of said channel region, a second gate (24) below said channel region; a first gate

dielectric (28) below said first gate, and a second gate dielectric (14) above said second gate, wherein the first gate and the second gate are electrically separated from each other, wherein the first gate comprises a different material than the second gate, wherein first gate, the second gate, and the channel region form a planarized structure, and wherein the first gate comprises a different thickness than the second gate.

2. The Pfiester Reference

Pfiester discloses a process for fabricating an isolated silicon-on-insulator (SOI) field effect transistor (FET) (10, 11, 13,15). The SOI FET is made on a substrate material (12). In one form, a first control electrode referred to as gate (24) is contained within the substrate (12) underlying a dielectric layer (14). A second control electrode referred to as gate (26) overlies a dielectric layer (28). A source and a drain current electrode are formed from a germanium-silicon layer (18). A silicon layer (16) forms an isolated channel region of the SOI FET. The gates (12, 24) are separated from the channel by gate dielectric layers (14, 28). The germanium-silicon layer (18) is much thicker than the silicon layer (16) which is made thin to provide a thin channel region. An optional nitride layer 20 overlies the germanium-silicon layer (18).

3. Applicants' Response

An important feature of the invention is that the double-gate structure is isolated from the underlying substrate. More specifically, as shown in Figures 47 and 48, the inventive structure includes an isolation layer 3 below the lower gate 22 (second gate). Independent claims 1 and 11 define this feature as follows: "an isolation layer below said second gate. . . ."

To the contrary, the structure disclosed in Pfiester is formed within a biased substrate 12. More specifically, the lower gate 24 is formed within the biased substrate 12. There is no isolation layer between the lower gate 24 and the biased substrate 12. Having one of the channels in direct contact with the substrate increases isolation-related problems such as latch-up and short channel effects. Therefore, Pfiester does not teach or suggest the invention as defined by independent claims 1 and 11, and does not anticipate independent claims 1 and 11. Further, dependent claims 4, 6-8, 14, and 18-20 are similarly not anticipated by Pfiester. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

B. The 35 U.S. C. §103(a) Rejection Based on Pfiester

1. The Position In the Office Action

With respect to the rejection of claims 2 and 12, the Office Action states that Pfiester teaches all claimed limitations as applied to claims 1 and 11 above. The Office Action recites that Pfiester fails to teach a doping concentration of the first and second gates. The Office

Action states that it is, however, well-known in the art to select the concentration of gates in devices. The Office Action declares that it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to have formed Pfiester's "first and second gate" using a different concentration, since it has held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involve only routine skills in the art. *In re Aller*, 105 USPQ 233.

The Office Action states that, with regard to the rejection of claims 3 and 13, Pfiester teaches all of the claimed limitations, as applied to claims 1 and 11 above, except for the species. The Office Action recites that it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to form the conductive layer, *having the materials as claimed*, since it has been held to be within the general skill of a worked in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

The argument in the Office Action regarding claims 9 and 15 states that Pfiester teaches all claimed limitations, as applied to claims 1 and 11 above, except that the first and second gate dielectrics comprise a different material. In the Office Action, it is stated that it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to form the dielectric layer, *having the materials as claimed*, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

Regarding claims 10 and 16, the Office Action asserts that Pfiester does not teach that the first and second gate dielectrics comprise a different thickness. The selection of thicknesses of various layers in device is an obvious design choice and, therefore is held within ordinary skills in the art.

2. Applicants' Response

As shown above, the structure disclosed in Pfiester is formed within a biased substrate 12. More specifically, the lower gate 24 is formed within the biased substrate 12. There is no isolation layer between the lower gate 24 and the biased substrate 12. Having one of the channels in direct contact with the substrate increases isolation-related problems such as latch-up and short channel effects. An important feature of the invention is that the double-gate structure is isolated from the underlying substrate. More specifically, as shown in Figures 47 and 48, the inventive structure includes an isolation layer 3 below the lower gate 22 (second gate). Independent claims 1 and 11 define this feature as follows: "an isolation layer below said second gate . . . ."

Therefore, Pfiester does not teach or suggest the invention as defined by independent claims 1 and 11 and independent claims 1 and 11 are patentable over Pfiester. In addition, dependent claims 2-3, 9-10, 12-13, and 15-16 are similarly patentable over Pfiester, not only by virtue of their dependency from a patentable independent claim, but also by virtue of the

additional features of the invention they define. In view the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

C. The 35 U.S. C. §103(a) Rejection Based on Pfiester in view of Uesugi

1. The Position In the Office Action

With regard to claims 5 and 17, the Office Action states that, although Pfiester fails to teach that the first conductive contact of a first gate and the second conductive contact of a second gate are coplanar, Uesugi teaches, in Fig. 1 and Col. 7, lines 42-46, the first conductive contact (80) of first gate (60) and the second conductive contact (90) of second gate (30) are coplanar. The Office Action argues, therefore, that it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to combine the teaching of Uesugi with Pfiester's device in order to reduce a manufacturing process.

2. The Uesugi Reference

Uesugi discloses a vertical semiconductor device having an insulated gate structure that makes use of a double-gate structure. The double-gate structure dramatically reduces the channel resistance, JFET resistance, and epitaxial resistance of the on-resistance of the power MOSFET, and implements an adequate breakdown voltage due to the effect of gate bias. In principle, a first gate and a second gate having mutually facing portions are driven synchronously. This causes

first and second channels to be formed in correspondence with the first and second gates, and the currents flowing through these first and second channels form the on-current for this power device having a vertical structure.

3. Applicants' Response

As discussed above, an important feature of the invention is that the double-gate structure is isolated from the underlying substrate. More specifically, as shown in Figures 47 and 48, the inventive structure includes an isolation layer 3 below the lower gate 22 (second gate). Independent claims 1 and 11 define this feature as follows: "an isolation layer below said second gate . . . ." To the contrary, the structure disclosed in Pfiester is formed within a biased substrate 12. More specifically, the lower gate 24 is formed within the biased substrate 12. There is no isolation layer between the lower gate 24 and the biased substrate 12. Having one of the channels in direct contact with the substrate increases isolation-related problems such as latch-up and short channel effects. Therefore, Pfiester does not teach or suggest the invention as defined by independent claims 1 and 11.

Uesugi does not cure the deficiencies of Pfiester. More specifically, Uesugi does not teach the double-gate structure defined by the claimed invention. The claimed invention includes a single channel between an upper gate and a lower gate. To the contrary, with the structure in Uesugi, two channel regions "Ch1" and "Ch2" are formed, one adjacent the first gate and another adjacent the second gate. Therefore, Uesugi is not in the same art field as the invention or

Pfiester (because Uesugi teaches multiple channel regions) and is not properly combinable with Uesugi to arrive at the claimed invention.

In addition, Uesugi does not teach or suggest the claimed "isolation layer below said second gate," as defined by independent claims 1 and 11. While Uesugi discloses a gate insulator GIS2 that surrounds the lower gate 30, this is not analogous to the claimed "isolation layer." An isolation layer completely separates the gate from any bias within an underlying substrate. To the contrary, a gate insulator is extremely thin and allows the substrate to have some biasing effect on an adjacent gate. Therefore, the usage of the term "isolation" in the claimed invention is an important feature that distinguishes the gate insulator "GIS2" of Uesugi from the claimed invention.

As shown above, Uesugi is not properly combinable with Pfiester and cannot render either independent claim 1 or 11 obvious. Further, even if one ordinarily skilled in the art would have combined Uesugi and Pfiester, the proposed combination would not teach or suggest the invention because neither reference teaches or suggests isolating the lower gate from the underlying substrate through the use of "an isolation layer below said second gate," as defined by independent claims 1 and 11. Therefore, independent claims 1 and 11 are patentable over the proposed combination of Uesugi and Pfiester. Further, dependent claims 5 and 17 are similarly patentable, not only by virtue of their dependency from a patentable independent claim, but also by virtue of the additional features of the invention they define. In view the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection

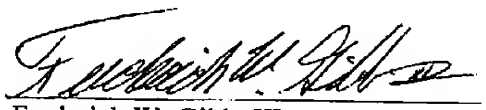
III. Formal Matters and Conclusion

In view of the foregoing, Applicants submit that claims 1-20, all the claims presently being examined in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary.

Please charge any deficiencies in fees and credit any overpayments to Attorney's Deposit Account Number 50-0510.

Respectfully submitted,



Frederick W. Gibb, III
Reg. No. 37,629

Dated: 11/30/01

McGinn & Gibb, PLLC
2568-A Riva Road, Suite 304
Annapolis, Maryland 21401
(410) 573-1545
Customer Number: 28211

IV. Marked Up Version of Claim Changes:

1. (Amended) A transistor comprising:

a channel region;

a first gate on top of said channel region;

a second gate below said channel region; and

an isolation layer below said second gate,

wherein said first gate and said second gate are electrically separated from each other.

11. (Amended) A semiconductor chip having at least one transistor, said transistor comprising:

a channel region;

a first gate on top of said channel region;

a second gate below said channel region; and

an isolation layer below said second gate,

wherein said first gate comprises a different material than said second gate.